REMARKS/ARGUMENTS

Before this Amendment, claims 1-3, 8-10, and 13-17 were present for examination. No additional claims have been cancelled. Claims 1-3, 8, 9, 15, and 16 are amended. No new claims are added. Before this Amendment, claims 14 and 17 already recited a "resolved" signal and a "resolved" node. Thus, a "resolved" value is not new matter. Because no new matter has been added, the amendments and addition do not necessitate a new search. Applicants respectfully request reconsideration of this application as amended.

The Office Action initially objected to claim 15 and rejected at least claim 1 and its dependent claims under 35 U.S.C. § 102 as being anticipated by SPICE 2G.1 User's Guide ("SPICE"). The Office Action also initially rejected claim 1 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 5,428,800 ("Hsieh"), rejected claim 2 under 35 U.S.C. § 103(a) as being unpatentable over Hsieh in view of U.S. Patent No. 5,202,593 ("Huang"), rejected claims 3, 8, and 16-17 under § 103(a) as being unpatentable over Hsieh, in view of U.S. Patent No. 4,922,445 ("Mizoue"), and rejected claims 9, 10, and 13-15 under § 103(a) as being unpatentable over Hsieh, in view of Mizoue and Huang.

In response to the final office action, an Amendment was submitted on July 18, 2006. That Amendment was not entered by the Office. In response, the following Amendment is submitted to address the remarks of the Examiner and reconsideration is respectfully requested. It is noted that claim 18 that was submitted in the July 18, 2006 response is not submitted as part of this response.

Claim Objections

The Office Action initially objected to claim 15. Claim 15 has been amended to clarify which values the claim refers to.

Patentability Requirements

The Advisory Action stated "applicant has amended and argued that the 'resolved value' is not taught by the prior art, but has nowhere pointed out how it is patentably

distinguishable from the prior art." The Applicant respectfully notes that "patentably distinguishable" is not an additional requirement for overcoming a rejection under 35 USC §102 or 103. Rather, it is believed that by addressing the §102 and §103 rejections as the Applicant has done below that the Applicant is satisfying the requirements of the Office and that no further showing is necessary.

35 U.S.C. § 102 Rejections, SPICE

Claim 1 has been amended to recite "a resolved value based upon at least the first value and second value." The Advisory action objected to the use of "resolved value" and indicated that its inclusion would require a new search. However, Applicants respectfully note that a "resolved" signal and a "resolved" node already existed in the claims prior to the issuance of the final office action and therefore would not require a new search. In addition, it is believed that "resolved signal" is a more narrow term than the term "third signal" which it replaces in claim 1 and therefore falls under the initial search that was conducted when "third signal" was searched as part of the initial examination. Therefore, it does not appear that a further search is required by the Office.

SPICE cannot support a bi-directional signal comprising a resolved value as recited in claim 1. Rather, the devices that SPICE can support are limited to DIODE, BJT, JFET, and MOSFET as shown on SPICE pages 30 to 37. In addition, according to SPICE page 1, SPICE only supports "**built-in** models for [these four] semiconductor devices." Consequently, SPICE discourages or at least does not teach or disclose **building a new** model of a device as shown in the present invention. Thus, it is clear that SPICE does not teach or disclose **modeling** a bi-directional signal comprising a resolved value as recited in claim 1.

The Office Action next suggested that "[s]ub-circuit design allows for **combination of models** to design complex circuits." However, the present invention reflects a **decomposition of one model**, namely a bi-directional signal of an electric circuit, into a first

value, a second value, and a resolved value. Even if SPICE teaches or discloses decomposition of one model, SPICE still fails to teach or disclose a resolved value.

Therefore, claim 1 and its dependent claims 2-3 are in condition for allowance because SPICE fails to teach or disclose modeling a bi-directional signal comprising a resolved value. Claims 8-10 and 13-17 are also in condition for allowance at least for the same reason.

35 U.S.C. § 102 Rejection, Hsieh

The Office Action also initially rejected claim 1 under 35 U.S.C. § 102(e) as being anticipated by Hsieh. The Office Action stated on page 3:

> "Hsieh '800 clearly teaches using FPGA (used in art for modeling circuits) to design input output interconnects. (Hsieh '800: Col. 1 Lines 25-37). FPGA as taught by Hsieh '800 shows a system for modeling interconnect or I/O (bidirectional) signals."

The Office Action also made similar remarks on pages 5-8. However, lines 49-54 of the cited column teach away from using FPGA to model a bi-directional signal:

> "While programmable FPGAs are very useful, they have some limitations. All input/output signals must be unidirectional, and all signals must be of the same logic level. Thus the FPGAs **cannot** be connected to bi-directional buses and cannot interface differing types of devices such as CMOS and TTL devices."

Thus, Hsieh does not teach or disclose using an FPGA to model a bi-directional signal. Even if Hsieh did teach or disclose using FPGA to model a bi-directional signal, nowhere in Hsieh does Hsieh teach or disclose **modeling** a bi-directional signal comprising a resolved value using a field programmable interconnect device ("FPID"). Rather, Hsieh teaches **implementing** a particular bi-directional buffer using FPID.

In addition, the particular bi-directional buffer that Hsieh implements is distinguishable from the present invention at least because Hsieh need not and does not teach or disclose a resolved value. The buffers in the present invention point **toward** each other and their outputs are **connected** to each other. However, as illustrated in Figure 4 of Hsieh and reproduced below, the buffers in Hsieh point **away** from each other and their outputs are **disconnected** from each other:

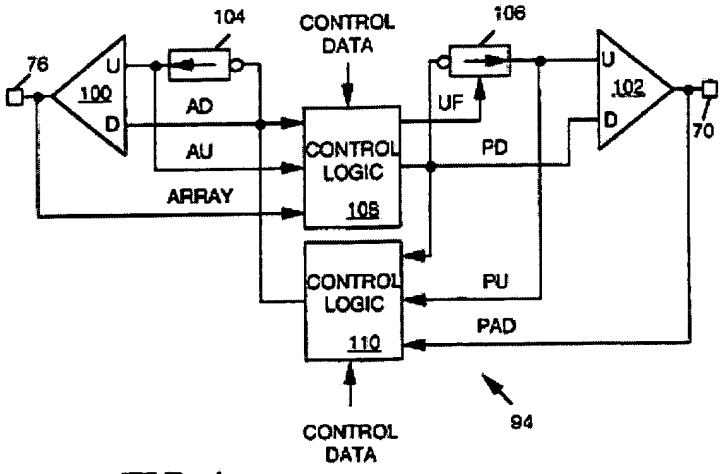


FIG. 4

Because the two buffers in Hsieh point **away** from each other and their outputs are **disconnected** from each other, Hsieh need not and does not teach or disclose a resolved value as recited in claim 1. The Office might contemplate construing single shot device 104 as generating a resolved value. However, Figure 4 clearly shows single shot device 104 as providing input into buffer 100, rather than receiving input from buffer 100 in order to generate a resolved value.

Therefore, claim 1 and its dependent claims 2-3 and 18 are in condition for allowance at least because Hsieh fails to teach or disclose modeling a bi-directional signal comprising a resolved value.

35 U.S.C. § 103 Rejection, Hsieh in view of Huang

The Office Action initially rejected claim 2 under 35 U.S.C. § 103(a) as being unpatentable over Hsieh in view of Huang. As noted previously, Hsieh fails to teach or disclose modeling a bi-directional signal comprising a resolved value. Also as noted previously, Hsieh teaches away from using FPGA to model a bi-directional signal. Thus, Hsieh fails to teach, disclose, or suggest modeling a bi-directional signal comprising a resolved value.

The combination of Hsieh with Huang fails to remedy Hsieh's deficiency. Nowhere in Huang does Huang teach, disclose, or suggest **modeling** a bi-directional signal comprising a resolved value. Rather, Huang is directed to **implementing** a bi-directional bus

repeater. Like Hsieh, the two buffers in Huang point **away** from each other and their output are **disconnected** from each other. Consequently, Huang need not and does not teach or disclose a resolved value.

Claim 2 has also been amended to recite "resistive data which models at least a portion of resistance coupled to an electric circuit." None of the references, alone or in combination, teaches, discloses, or suggests "resistance **coupled** with said electric circuit" as recited in claim 2. Rather, the only reference of resistance is the internal resistor **contained within** buffer 16 as shown in Figure 2 of Huang. An internal resistor that is **contained within** a buffer is clearly not resistance **coupled** with an electric circuit.

Therefore, claim 2 is also allowable because none of the references, alone or in combination, teaches, discloses, or suggests every element of claim 2.

35 U.S.C. § 103 Rejections, Hsieh in view of Mizoue

The Office Action initially rejected claims 3, 8, and 16-17 under § 103(a) as being unpatentable over Hsieh in view of Mizoue. As noted previously, Hsieh fails to teach, disclose, or suggest modeling a bi-directional signal comprising a resolved value. The Mizoue reference fails to remedy Hsieh's deficiency. Not only does Mizoue fail to teach, disclose, or suggest modeling a bi-directional signal comprising a resolved value but also Mizoue is from a different field. The Office Action recognizes on page 2 in referring to the SpiceI reference that the presently claimed invention is dircted at modeling analog circuits. Namely, the Office Action stated: "Model Card describing a model and having various levels of input and out[put] as [an] **analog circuit**" because the present claimed invention involves an analog circuit. However, Mizoue is directed to a **logic circuit** simulation method. Thus, the combination is not operable to generate a resolved value of an analog circuit.

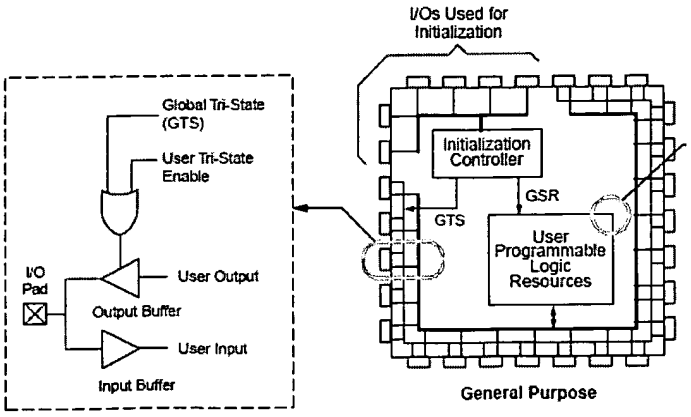
Claim 8 recites a method for modeling a bi-directional signal comprising a resolved value of claim 1. Likewise, claim 16 recites a method for operating an improved pad cell model based on claim 1. Therefore, just like claim 1 is allowable, both claims 8 and 16 are allowable because none of the references, alone or in combination, teaches, discloses, or suggests

every element of each claim. Accordingly, claims 3 and 17 are each allowable for being dependent from an allowable independent claim.

35 U.S.C. § 103 Rejections, Hsieh in view of Mizoue and Huang

The Office Action initially rejected claims 9, 10, and 13-15 under § 103(a) as being unpatentable over Hsieh, in view of Mizoue and Huang. As noted previously, neither Mizoue nor Huang remedy Hsieh's deficiency. Also as noted previously, claim 8 is allowable because none of the references, alone or in combination, teaches, discloses, or suggests a bi-directional signal comprising a resolved value. Claims 9-10 are thus allowable for being dependent from allowable independent claim 8. Claims 14-15 are likewise allowable because none of the references, alone or in combination, teaches, discloses, or suggests a bi-directional signal comprising a resolved value.

Claims 9, 10, and 13-15 are also allowable for reciting additional elements that none of the references, alone or in combination, teaches, discloses, or suggests. Claim 9 recites in part a "pad cell." Both claims 13 and 15 recite in part a "bi-directional pad." However, none of the references, alone or in combination, teaches, discloses, or suggests a bi-directional pad or an I/O pad. Rather, Hsieh and Huang are directed to input/output buffers. Input/output **buffers** are clearly distinguishable from an I/O **pad**. For example, as illustrated on page 9 of "HDL Simulation Using the Xilinx Alliance Series Software" (see accompanying Information Disclosure Statement) and shown below, the edge of a field programmable device is likely to comprise an I/O Pad, an Input Buffer, and an Output Buffer:



Despite their proximity to each other, input/output **buffers** are not an I/O **pad**. For example, as noted previously, input/output buffers point **away** from each other and their output are **disconnected** from each other. However, the buffers in the present I/O pad model point **toward** each other and their output are **connected** to each other.

Because input/output **buffers** are clearly distinguishable from an I/O **pad**, Hsieh and Huang do not teach, disclose, or suggest modeling a pad cell or a bi-directional pad. As noted previously, Hsieh or Huang teach **implementing** their particular input/output **buffers**. However, even if Hsieh or Huang's teachings of **implementing** input/output **buffers** could be construed as teachings of **modeling** input/output **buffers**, Hsieh and Huang still do not teach, disclose, or suggest **modeling** a **pad** cell or a bi-directional **pad**.

Moreover, as noted previously, Mizoue is directed to a **logic circuit** simulation method. A logic circuit comprises logic devices such as AND or XOR gates. However, buffers and a bi-directional pad are not logic devices as they do not perform any logic. Thus, even if Hsieh and Huang do teach modeling input/output buffers or even a bi-directional pad, Mizoue's teaching of **logic circuit** simulation and storing the simulation results is not combinable with input/output buffers or even a bi-directional pad.

It is believed that reference to "HDL Simulation Using the Xilinx Alliance Series Software" does not create any further need for searching as the reference is included in the attached information disclosure statement and the concept of an I/O pad is readily comprehendable by an examiner.

Therefore, claims 9, 10, and 13-15 are allowable because none of the references, alone or in combination, teaches, discloses, or suggests every element of each claim.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance and an action to that end is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 303-571-4000.

Respectfully submitted,

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